ABSTRACT OF THE DISCLOSURE

A phase locked loop, PLL, is described with multiple parallel **chnrge** pumps that are selectively disabled as phase lock is approached. A lock detection circuit is described that enabled reference currents to be fed to the parallel charge pumps. The error signal from a phase detector is arranged as UP and a DOWN signals that are averaged in the lock detector. When the average error is large, all the reference currents feed the charge pumps that provide a high loop gain to reduce the lock time. As the lock becomes closer selective reference currents are disabled to reduce loop gain so that a smooth transition to lock is made. Selectively switching currents into a low pass filter that usually follows a charge pump in a PLL circuit automatically reduces switching noise by the operation of the low pass filter.